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174/301

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : David Mendel et al.

Application No. : 10/796,501 Confirmation No.: 3005

Filed : March 8, 2004

For : SYSTEMS AND METHODS FOR REDUCING STATIC AND TOTAL POWER CONSUMPTION IN A PROGRAMMABLE LOGIC DEVICE

Group Art Unit : 2819

New York, New York 10020
September 28, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants hereby make the following references of record in the above-identified patent application:

U.S. Patents

6,407,576	Ngai et al.	6/18/02

Other Documents

Jason H. Anderson and Farid N. Najm, "A Novel Low-Power FPGA Routing Switch" (2004) (unpublished, submitted to the 2004 IEEE Custom Integrated Circuits Conference, Orlando, Florida, October 3-6, 2004).

Jason H. Anderson et al., "Active Leakage Power Optimization for FPGAs", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 33-41 (February 22-24, 2004).

Jason H. Anderson and Farid N. Najm, "Low-Power Programmable Routing Circuitry for FPGAs" (2004) (unpublished, submitted to the 2004 International Conference on Computer Aided Design, San Jose, California, November 7-11, 2004).

Deming Chen and Jason Cong, "Low-Power Technology Mapping for FPGA Architectures with Dual Supply Voltages", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 109-117 (February 22-24, 2004).

A. Gayasen et al., "Reducing Leakage Energy in FPGAs Using Region-Constrained Placement", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 51-58 (February 22-24, 2004).

Fei Li et al., "Low-Power FPGA Using Pre-defined Dual-Vdd/Dual-Vt Fabrics", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 42-50 (February 22-24, 2004).

Fei Li et al., "FPGA Power Reduction Using Configurable Dual-Vdd", 2004 Design Automation Conference, San Diego, California, pp. 735-740 (June 7-11, 2004).

Arifur Rahman and Vijay Polavarapuv, "Evaluation of Low-Leakage Design Techniques for Field Programmable Gate Arrays", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 23-30 (February 22-24, 2004).

"Mercury Programmable Logic Device Family", Data Sheet, Version 2.2, Altera Corporation, pp. 17-28 (January 2003).

Copies of the aforementioned references, which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

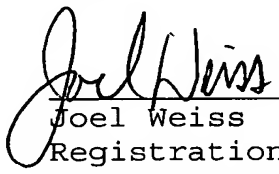
It is respectfully requested that these references be (1) fully considered by the Patent and Trademark Office during examination of this application;

and (2) printed on any patent which may issue on this application. Applicants request that a copy of Form PTO-1449, as considered and initialed by the Examiner, be returned with the next communication.

In accordance with 37 C.F.R. § 1.97, submission of this Statement requires no fee. However, if for any reason a fee is due, the Director of the United States Patent and Trademark Office is hereby authorized to charge payment of any fees required in connection with this Information Disclosure Statement to Deposit Account No. 06-1075. A duplicate copy of this Statement is transmitted herewith.

An early and favorable action is respectfully requested.

Respectfully submitted,



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I hereby certify that this Correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope Addressed to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 on

September 28, 2004

Claire J. Sullivan Goodman

Signature of Person Signing

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 174/301	APPLICATION NO. 10/796,501
INFORMATION DISCLOSURE STATEMENT BY APPLICANTS	APPLICANTS David Mendel et al.	CONFIRMATION NO. 3005
	FILING DATE March 8, 2004	GROUP ART UNIT 2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6,407,576	6/18/02	Ngai et al.	326	41	

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
	Jason H. Anderson and Farid N. Najm, "A Novel Low-Power FPGA Routing Switch" (2004) (unpublished, submitted to the 2004 IEEE Custom Integrated Circuits Conference, Orlando, Florida, October 3-6, 2004).
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EXAMINER **DATE CONSIDERED**

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicants.

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